the protuberances. In some embodiments, relatively weak couplings of the semiconductor substrates to the protuberances may be broken or severed. Notice that in the illustration, the protuberances remain behind still coupled with the substrate. In other embodiments this may not be the case, as will be discussed further below (e.g., the protuberances may remain connected to the semiconductor devices).

**[0039]** In some embodiments, the separation of the receiving substrate **226** from the substrate **212** may involve a wafer-level lift off of multiple or potentially many semiconductor devices **216** across the length of the substrate **212**. In some embodiments, all of the semiconductor devices **216** may be lifted off in one such lift-off operation with one receiving substrate. Alternatively, different groups or subsets of the semiconductor devices **216** may be Idled off during different lift-off operations with different receiving substrates. For example, two, three, or four, or more of such lift-off operations may be used to separate substantially all of the semiconductor devices from off the substrate. In some embodiments, rigid receiving substrate(s) may be used. In other embodiments, flexible receiving substrate(s) may be used. In some embodiments, flexible receiving substrate(s) that are substantially puncture proof may optionally be used, although this is not required.

**[0040]** It is to be appreciated that the scope of the invention is not limited to the particular method and substrates/objects described above. The method of FIG. **1** and the approach of FIGS. **2**A-**2**C have been shown and described in a relatively basic form, but additional operations may optionally be added and/or certain operations may be removed. For example, in an alternate embodiment, the method of FIG. **1** may optionally omit the operation of block **101** and/or **104**. For example, the operation of block **104** may be performed by another entity, at another facility, etc. In other embodiments, various other operations disclosed elsewhere herein may optionally be added to the operations of Figure and/or FIGS. **2**A-**2**C (e.g., anchors may be formed, substrates may be regenerated, etch openings may be formed, etch stop layers may be deposited, etc.).

**[0041]** FIGS. **3**A-**3**I are cross-sectional side views of embodiments of workpiece objects at different stages of an embodiment of an approach for separating group III-V compound semiconductor devices from a substrate by etching a graded composition group III-V compound semiconductor release layer **314**. In some embodiments, the workpiece objects may be used in the method of FIG. **1**. The components, features, and optional details described for any of the workpiece objects of FIGS. **3**A-**3**I also optionally apply to the operations and/or method of FIG. **1**. However, it is to be appreciated that the operations and/or method of FIG. **1** may be used with different workpiece objects than those of FIGS. **3**A-**3**I. Moreover, the workpiece objects of FIGS. **3**A-**3**I may be used with different operations and/or a different method than that of FIG. **1**.

**[0042]** FIG. **3**A shows an embodiment eta workpiece object **310**A having a substrate **311**, and a group III-V compound semiconductor layer **312**. For simplicity, the group III-V compound semiconductor layer may also be referred to herein simply as the group III-V layer. A dashed line between the substrate and the group III-V layer is used to indicate that, in some embodiments, the substrate may be a group III-V compound semiconductor substrate of which the group III-V layer is an uppermost portion. This often tends to provide high quality device layers due to the lattice match of the group III-V layer with the substrate. Such a group III-V compound semiconductor substrate often tends to be relatively costly due in part to the hulk group III-V compound semiconductor material needed to provide mechanical support, although the substrates may optionally be reused to help reduce costs, as will be disclosed further below. As another option, in some embodiments, the group III-V layer may be formed as a discrete layer on or over the substrate which is not a group III-V compound semiconductor substrate, but rather some other type of material. For example, the substrate may be a silicon substrate, a ceramic substrate, a glass substrate, a perforated substrate, or various other types of substrates less costly per unit material than group III-V compound semiconductor materials. The group III-V layer may either be formed directly on the substrate provided there is sufficient lattice matching, or one or more intervening lattice matching layers or buffer layers may be formed over the substrate between the substrate and the group III-V layer. Using such substrates may tend to be more cost effective, since relatively costly group III-V compound semiconductor materials do not need to be used to provide mechanical support that can instead be provided by more cost effective materials.

**[0043]** A graded composition group III-V compound semiconductor release layer **314** is formed on and/or over the group III-V layer **312**. For simplicity, the graded composition group III-V compound semiconductor release layer may also be referred to herein as the graded composition release layer, the group III-V release layer, or simply the release layer. In some embodiments, the graded composition release layer may be lattice matched to the underlying group III-V layer and/or another layer on which it is formed, if this is needed for the particular implementation. As before, a composition of at least one component may be graded across a thickness of the graded composition release layer. Linear or non-linear gradual/continuous gradations, discrete or stepwise gradations, or a combination thereof, may optionally be used. In some embodiments, the graded composition release layer may have a thickness ranging from about 200 Å to about 10 μm, or in some cases from about 500 Å to about 5 μm, although the scope of the invention is not so limited. In one example embodiment, the graded composition release layer may be a graded indium-gallium-arsenide-phosphorous (InGaAsP) to indium-gallium-arsenide (InGaAs) layer. In some embodiments, the graded composition may modify an etch rate of a given etch. The gradation in the composition may change an etch rate of an etch used to etch the graded composition release layer, as will be explained further below. Any gradation operable to form the protuberances and/or non-flat surfaces discussed elsewhere herein during the etch should generally be suitable.

**[0044]** A set of group III-V compound semiconductor device layers **330** are formed over and/or on the graded composition release layer **314**. For simplicity, the group III-V compound semiconductor device layers may also be referred to herein simply as the group III-V device layers. The group III-V device layers include a lower contact layer **332**, a set of one or more group III-V compound semiconductor device active layers **336** (for simplicity also referred to herein simply as the group III-V device active layers) formed over and/or on the lower contact layer, and an upper contact layer **336** formed over and/or on the set of group III-V compound semiconductor device active layers. In some embodiments, the upper and lower contact layers may represent semiconductor layers that are latticed matched to their interfacing